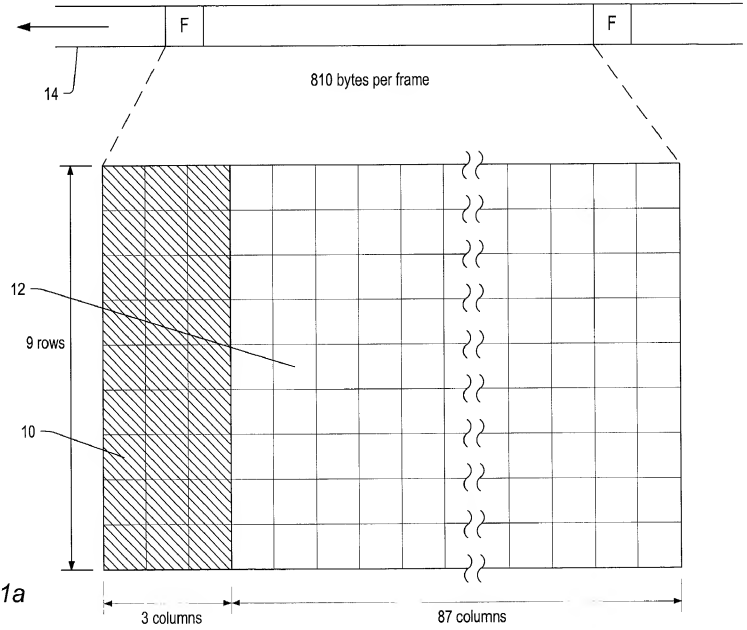

FIG. 1a

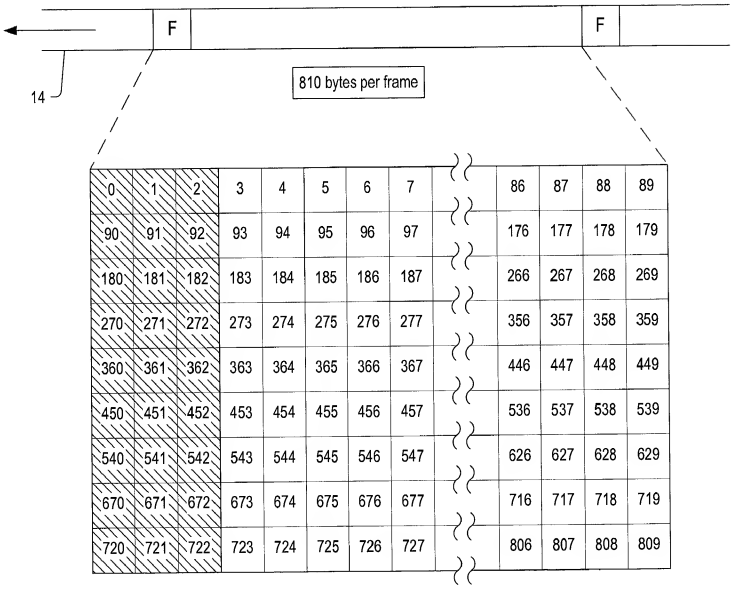
F
F
14
810 bytes per frame
0 1 2 3 4 5 6 7 86 87 88 89
90 91 92 93 94 95 96 97 176 177 178 179
180 181 182 183 184 185 186 187 266 267 268 269
270 271 272 273 274 275 276 277 356 357 358 359
360 361 362 363 364 365 366 367 446 447 448 449
450 451 452 453 454 455 456 457 536 537 538 539
540 541 542 543 544 545 546 547 626 627 628 629
670 671 672 673 674 675 676 677 716 717 718 719
720 721 722 723 724 725 726 727 806 807 808 809

FIG. 1b

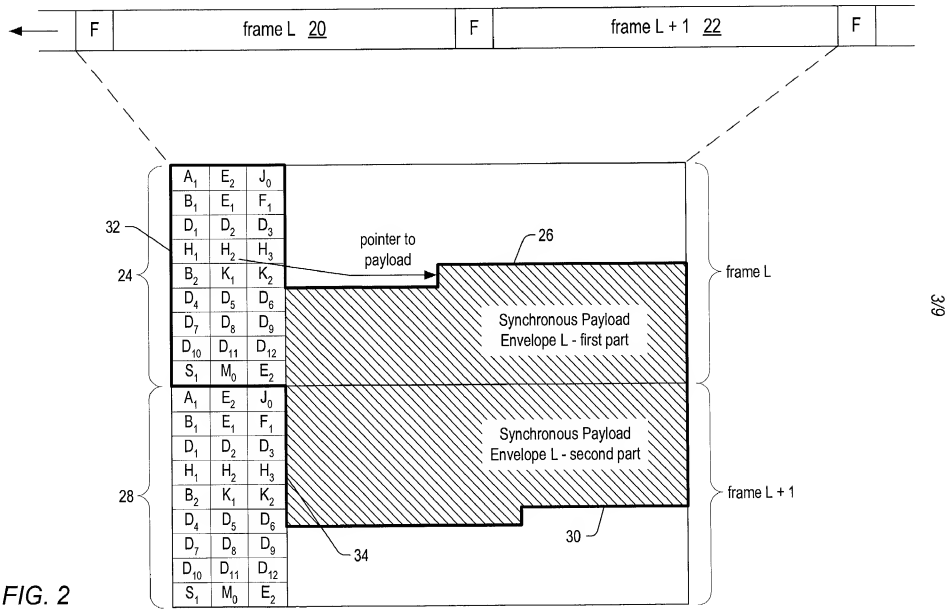
F
frame L 20
F
frame L + 1 22
F
32
24
28
pointer to payload
26
Synchronous Payload Envelope L - first part
Synchronous Payload Envelope L - second part
frame L
frame L + 1
30
34
A1 E2 J0
B1 E1 F1
D1 D2 D3
H1 H2 H3
B2 K1 K2
D4 D5 D6
D7 D8 D9
D10 D11 D12
S1 M0 E2

FIG. 2

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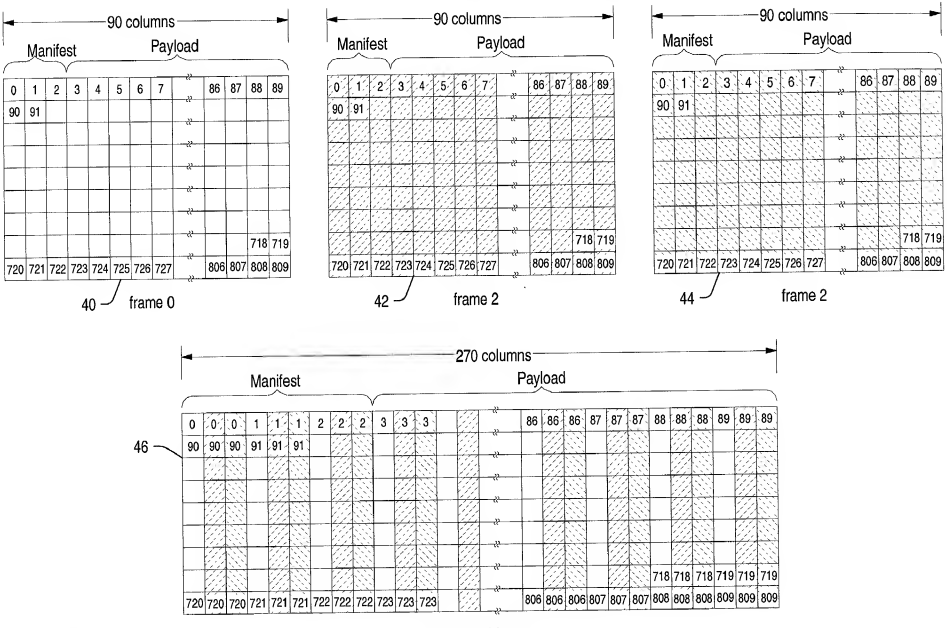

FIG. 3

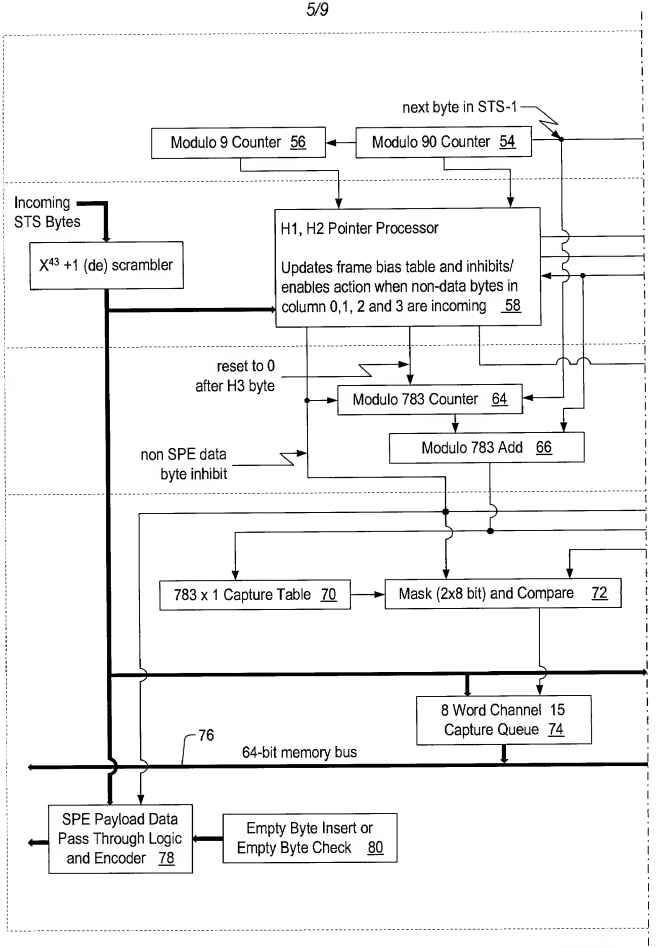
next byte in STS-1
Modulo 9 Counter 56
Modulo 90 Counter 54
Incoming STS Bytes
X43 +1 (de) scrambler
H1, H2 Pointer Processor
Updates frame bias table and inhibits/ enables action when non-data bytes in column 0,1, 2 and 3 are incoming 58
reset to 0 after H3 byte
Modulo 783 Counter 64
Modulo 783 Add 66
non SPE data byte inhibit
783 x 1 Capture Table 70
Mask (2x8 bit) and Compare 72
8 Word Channel 15 Capture Queue 74
76
64-bit memory bus
SPE Payload Data Pass Through Logic and Encoder 78
Empty Byte Insert or Empty Byte Check 80

FIG. 4a

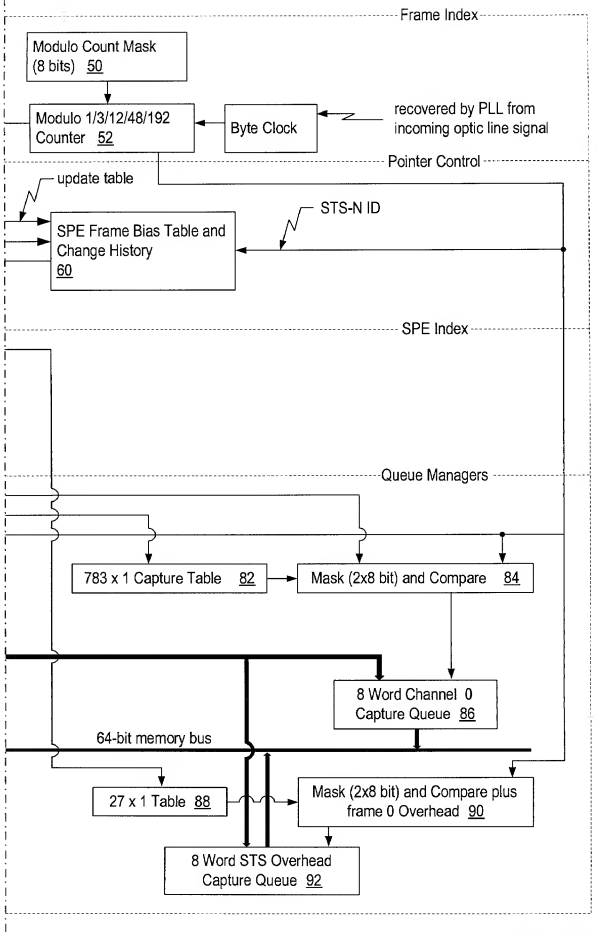
Frame Index
Modulo Count Mask (8 bits) 50
Modulo 1/3/12/48/192 Counter 52
Byte Clock
recovered by PLL from incoming optic line signal
Pointer Control
update table
STS-N ID
SPE Frame Bias Table and Change History 60
SPE Index
Queue Managers
783 x 1 Capture Table 82
Mask (2x8 bit) and Compare 84
8 Word Channel 0 Capture Queue 86
64-bit memory bus
27 x 1 Table 88
Mask (2x8 bit) and Compare plus frame 0 Overhead 90
8 Word STS Overhead Capture Queue 92

FIG. 4b

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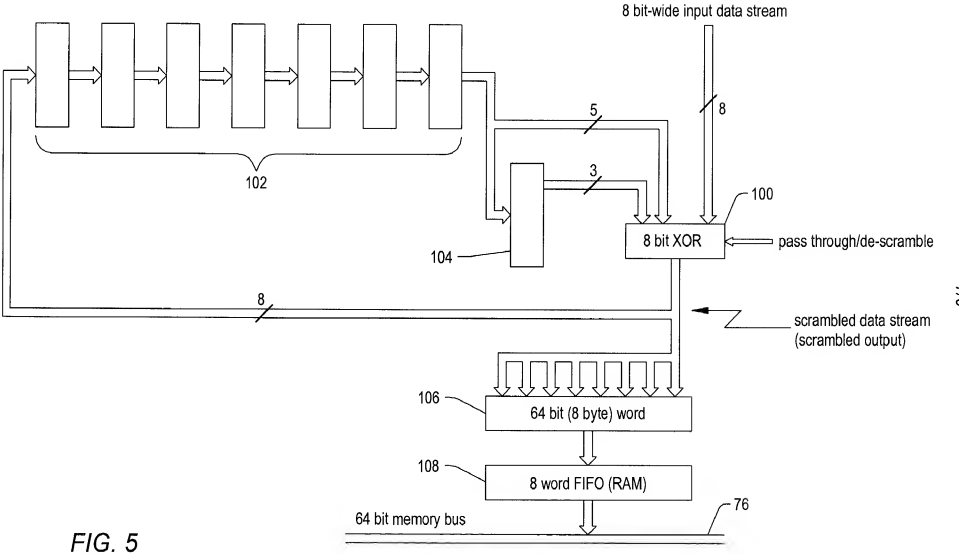

FIG. 5

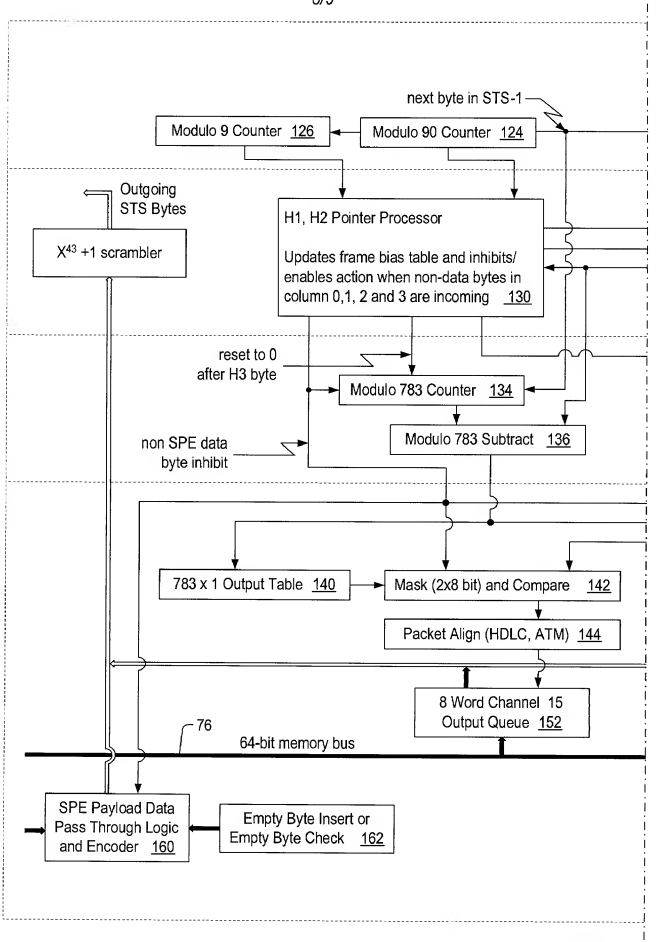
next byte in STS-1
Modulo 9 Counter 126
Modulo 90 Counter 124
Outgoing STS Bytes
X43 +1 scrambler
H1, H2 Pointer Processor
Updates frame bias table and inhibits/ enables action when non-data bytes in column 0,1, 2 and 3 are incoming 130
reset to 0 after H3 byte
Modulo 783 Counter 134
non SPE data byte inhibit
Modulo 783 Subtract 136
783 x 1 Output Table 140
Mask (2x8 bit) and Compare 142
Packet Align (HDLC, ATM) 144
8 Word Channel 15 Output Queue 152
76
64-bit memory bus
SPE Payload Data Pass Through Logic and Encoder 160
Empty Byte Insert or Empty Byte Check 162

FIG. 6a

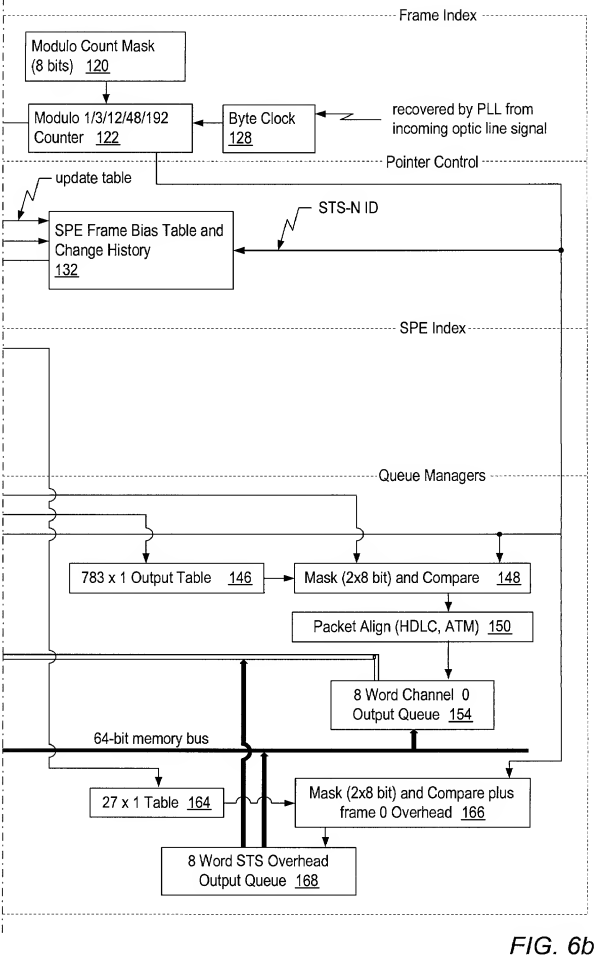
Frame Index
Modulo Count Mask (8 bits) 120
Modulo 1/3/12/48/192 Counter 122
Byte Clock 128
recovered by PLL from incoming optic line signal
Pointer Control
update table
STS-N ID
SPE Frame Bias Table and Change History 132
SPE Index
Queue Managers
783 x 1 Output Table 146
Mask (2x8 bit) and Compare 148
Packet Align (HDLC, ATM) 150
8 Word Channel 0 Output Queue 154
64-bit memory bus
27 x 1 Table 164
Mask (2x8 bit) and Compare plus frame 0 Overhead 166
8 Word STS Overhead Output Queue 168

FIG. 6b